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EXAMINER

LEWIS, MONICA

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 04/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/017,737	ANO, KAZUAKI	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 January 2003.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 and 21-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 21-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 December 2001 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
     If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \* c) ☐ None of:  
         1. ☐ Certified copies of the priority documents have been received.  
         2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
     \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
     a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3</u> . | 6) <input type="checkbox"/> Other: _____                                    |

### **DETAILED ACTION**

1. This action is in response to the amendment filed January 29, 2003.

#### ***Response to Arguments***

2. Applicant's arguments with respect to claims 1-10 and 21-30 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Specification***

3. The title of the invention is not **descriptive**. A new title is required that is clearly indicative of the invention to which the claims are directed.

#### ***Drawings***

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "substrate having a plurality of contact pads must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

#### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. Claims 1-5 and 21 are rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art in view of Takiar et al. (U.S. Patent No. 5,495,398) and LoBianco et al. (U.S. Patent No. 6,340,846).

In regards to claim 1, Applicant's Prior Art discloses the following:

a) a first chip (10) having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire (See Figure 1 and Page 2 Lines 7 and 8); and

b) a second chip (30) having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire (See Figure 1 and Page 2 Lines 7 and 8).

In regards to claim 1, Applicant's Prior Art fails to disclose the following:

a) a first attach layer having an area equal to an area of said second chip bottom surface for coupling said first chip and said second chip, said first attach layer having a thickness to provide electrical disconnection of said first chip wire bonds and said second chip, said first attach layer is applied to said second chip bottom surface prior to coupling said first chip and said second chip.

However, Takiar et al. ("Takiar") discloses the use of attach areas that have the same area as the chip (See Figure 1 and Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of attach areas that have the same area as the chip as disclosed in Takiar because they aid in providing an electrical connection among the various components (See Figure 1 and Figure 3).

Additionally, since Applicant's Prior Art and Takiar are both from the same field of endeavor, the purpose disclosed by Takiar would have been recognized in the pertinent art of Applicant's Prior Art.

b) attach layer covering each of said bonding pads on said first chip.

However, LoBianco et al. ("LoBianco") discloses the use of an attach layer to cover a bonding pad (See Figure 3 and Figure 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of an attach layer to cover a bonding pad as disclosed in LoBianco because it aids in preventing bending or breakage of the bonds (See Column 2 Lines 23-55).

Additionally, since Applicant's Prior Art and LoBianco are both from the same field of endeavor, the purpose disclosed by LoBianco would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 2, Applicant's Prior Art fails to disclose the following:

a) electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately 10  $\mu\text{m}$ .

However, the applicant has not established the critical nature of the dimension of 10  $\mu\text{m}$ . "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 3, Applicant's Prior Art fails to disclose the following:

a) first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond.

However, Takiar discloses the use of a thermosetting material (See Column 5 Lines 38-52). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of thermosetting material as disclosed in Takiar because it aids in providing an connection among the chips (See Column 5 Lines 38-52).

Additionally, since Applicant's Prior Art and Takiar are both from the same field of endeavor, the purpose disclosed by Takiar would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 4, Applicant's Prior Art discloses the following:

a) first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas (See Figure 1).

In regards to claim 5, Applicant's Prior Art discloses the following:

a) first chip and said second chip have a stacked arrangement such that said first chip bonding pads are covered from above by said second chip (See Figure 1 and Page 2 Lines 7 and 8).

In regards to claim 21, Applicant's Prior Art discloses the following:

a) a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface (See Figure 1 and Page 2 Lines 7 and 8);

b) a wire having a bond to one of said first bonding pads (See Figure 1); and

c) a second chip having opposing top and bottom surfaces and positioned with said bottom surface adjacent said top surface of said first chip (See Figure 1 and Page 2 Lines 7 and 8).

In regards to claim 21, Applicant's Prior Art fails to disclose the following:

a) a first attach layer between said top surface of said first chip and said bottom surface of said second chip, said first attach area having an area substantially equal to the are of said second chip.

However, Takiar discloses the use of attach areas that have the same area as the chip (See Figure 1 and Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of attach areas that have the same area as the chip as disclosed in Takiar because they aid in providing an electrical connection among the various components (See Figure 1 and Figure 3).

Additionally, since Applicant's Prior Art and Takiar are both from the same field of endeavor, the purpose disclosed by Takiar would have been recognized in the pertinent art of Applicant's Prior Art.

b) attach layer covering said wire bond.

However, LoBianco discloses the use of an attach layer to cover a wire bond (See Figure 3 and Figure 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of an attach layer to cover a wire bond as disclosed in LoBianco because it aids in preventing bending or breakage of the bonds (See Column 2 Lines 23-55).

Additionally, since Applicant's Prior Art and LoBianco are both from the same field of endeavor, the purpose disclosed by LoBianco would have been recognized in the pertinent art of Applicant's Prior Art.

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7. Claims 6, 8-10, 22, 23 and 25 are rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art in view of Takiar et al. (U.S. Patent No. 5,495,398), LoBianco et al. (U.S. Patent No. 6,340,846) and Fogal et al. (U.S. Patent No. 5,323,060).

In regards to claim 6, Applicant's Prior Art fails to disclose the following:

a) a second attach layer having an area equal to said second chip bottom surface area and disposed between said first attach layer and said second chip bottom surface, said second attach layer being an insulating material having a thickness cooperable with said first attach layer to provide electrical disconnection of said first chip wire bonds and said second chip.

However, Takiar discloses the use of attach areas that have the same area as the chip (See Figure 1 and Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of attach areas that have the same area as the chip as disclosed in Takiar because they aid in providing an electrical connection among the various components (See Figure 1 and Figure 3).

Additionally, since Applicant's Prior Art and Takiar are both from the same field of endeavor, the purpose disclosed by Takiar would have been recognized in the pertinent art of Applicant's Prior Art.

However, Fogal et al. ("Fogal") discloses the use of a second attach layer adjacent to said bottom surface of said second chip (See Figure 1 and Column 3 Lines 13-29). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of use of a second attach layer adjacent to said bottom surface of said second chip as the chip as disclosed in Fogal because it aids in providing an electrical connection among the various components (See Figure 1).



Additionally, since Applicant's Prior Art and Fogal are both from the same field of endeavor, the purpose disclosed by Fogal would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 8, Applicant's Prior Art discloses the following:

a) electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately equal to said second attach layer thickness (See Figure 1).

In regards to claim 9, Applicant's Prior Art fails to disclose the following:

a) second attach layer thickness is approximately 1  $\mu\text{m}$ .

However, the applicant has not established the critical nature of the dimension of 1  $\mu\text{m}$ . "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 10, Applicant's Prior Art discloses the following:

a) first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas, and wherein said first and second chips are stacked such that said first chip bonding pads are covered from above by said second chip (See Figure 1).

In regards to claim 22, Applicant's Prior Art fails to disclose the following:

a) a second attach layer adjacent to said bottom surface of said second chip.

However, Fogal discloses the use of a second attach layer adjacent to said bottom surface of said second chip (See Figure 1 and Column 3 Lines 13-29). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the

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semiconductor device of Applicant's Prior Art to include the use of use of a second attach layer adjacent to said bottom surface of said second chip as the chip as disclosed in Fogal because it aids in providing an electrical connection among the various components (See Figure 1).

Additionally, since Applicant's Prior Art and Fogal are both from the same field of endeavor, the purpose disclosed by Fogal would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 23, Applicant's Prior Art fails to disclose the following:

- a) first attach layer is a thermosetting material.

However, Takiar discloses the use of a thermosetting material (See Column 5 Lines 38-52). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of thermosetting material as disclosed in Takiar because it aids in providing an connection among the chips (See Column 5 Lines 38-52).

Additionally, since Applicant's Prior Art and Takiar are both from the same field of endeavor, the purpose disclosed by Takiar would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 25, Applicant's Prior Art discloses the following:

- a) the first and second chips are approximately the same size (See Figure 1).

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8. Claims 7 and 24 are rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art in view of Takiar et al. (U.S. Patent No. 5,495,398), LoBianco et al. (U.S. Patent No. 6,340,846), Fogal et al. (U.S. Patent No. 5,323,060) and Kuramochi (U.S. Patent No. 5,521,122).

In regards to claim 7, Applicant's Prior Art fails to disclose the following:

a) thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond.

However, Takiar discloses the use of a thermosetting material (See Column 5 Lines 38-52). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of thermosetting material as disclosed in Takiar because it aids in providing an connection among the chips (See Column 5 Lines 38-52).

Additionally, since Applicant's Prior Art and Takiar are both from the same field of endeavor, the purpose disclosed by Takiar would have been recognized in the pertinent art of Applicant's Prior Art.

b) second attach layer is silicon dioxide.

However, Kuramochi discloses the use of silicon dioxide (See Column 5 Lines 28-31). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of silicon dioxide as disclosed in Kuramochi because it is usable in accordance with a kind of material and hardening temperature for an insulating film (See Column 5 Lines 25-39).

Additionally, since Applicant's Prior Art and Kuramochi are both from the same field of endeavor, the purpose disclosed by Kuramochi would have been recognized in the pertinent art of Applicant's Prior Art.

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In regards to claim 24, Applicant's Prior Art fails to disclose the following:

- a) second attach layer is an inorganic material.

However, Kuramochi discloses the use of silicon dioxide (See Column 5 Lines 28-31). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of silicon dioxide as disclosed in Kuramochi because it is usable in accordance with a kind of material and hardening temperature for an insulating film (See Column 5 Lines 25-39).

Additionally, since Applicant's Prior Art and Kuramochi are both from the same field of endeavor, the purpose disclosed by Kuramochi would have been recognized in the pertinent art of Applicant's Prior Art.

9. Claims 26-29 are rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art in view of Takiar et al. (U.S. Patent No. 5,495,398), LoBianco et al. (U.S. Patent No. 6,340,846) and Tuckerman et al. (U.S. Patent No. 5,804,004).

In regards to claim 26, Applicant's Prior Art discloses the following:

- a) a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface, said first chip mounted on said substrate (See Figure 1 and Page 2 Lines 7 and 8);

- b) a wire having a ball bond (See Figure 1 and Specification Page 8 Line 5);

- c) a second chip having opposing top and bottom surfaces and positioned with said bottom surface of said second chip adjacent said top surface of said first chip (See Figure 1 and Page 2 Lines 7 and 8).

In regards to claim 26, Applicant's Prior Art fails to disclose the following:

- a) a first attach layer between said top surface of said first chip and said bottom surface of said second chip and covering said wire bond to said one of said first bonding pads, said first attach layer having an area substantially equal to the area of said second chip.

However, Takiar discloses the use of attach areas that have the same area as the chip (See Figure 1 and Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of attach areas that have the same area as the chip as disclosed in Takiar because they aid in providing an electrical connection among the various components (See Figure 1 and Figure 3).

Additionally, since Applicant's Prior Art and Takiar are both from the same field of endeavor, the purpose disclosed by Takiar would have been recognized in the pertinent art of Applicant's Prior Art.

b) attach layer covering each of said bonding pads on said first chip.

However, LoBianco et al. ("LoBianco") discloses the use of an attach layer to cover a bonding pad (See Figure 3 and Figure 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of an attach layer to cover a bonding pad as disclosed in LoBianco because it aids in preventing bending or breakage of the bonds (See Column 2 Lines 23-55).

Additionally, since Applicant's Prior Art and LoBianco are both from the same field of endeavor, the purpose disclosed by LoBianco would have been recognized in the pertinent art of Applicant's Prior Art.

c) a substrate having a plurality of contact pads.

However, Tuckerman discloses the use of a substrate with a plurality of contact pads (See Figure 4a). It would have been obvious to one having ordinary skill in the art at the time the

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invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of a substrate having a plurality of contact pads as disclosed in Tuckerman because it aids in providing a connection among the various components (See Figure 4a).

Additionally, since Applicant's Prior Art and Tuckerman are both from the same field of endeavor, the purpose disclosed by Tuckerman would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 27, Applicant's Prior Art fails to disclose the following:

a) a second attach layer adjacent to said bottom surface of said second chip.

However, Fogal discloses the use of a second attach layer adjacent to said bottom surface of said second chip (See Figure 1 and Column 3 Lines 13-29). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of use of a second attach layer adjacent to said bottom surface of said second chip as the chip as disclosed in Fogal because it aids in providing an electrical connection among the various components (See Figure 1).

Additionally, since Applicant's Prior Art and Fogal are both from the same field of endeavor, the purpose disclosed by Fogal would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 28, Applicant's Prior Art fails to disclose the following:

a) first attach layer is a thermosetting material.

However, Takiar discloses the use of a thermosetting material (See Column 5 Lines 38-52). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the

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use of thermosetting material as disclosed in Takiar because it aids in providing an connection among the chips (See Column 5 Lines 38-52).

Additionally, since Applicant's Prior Art and Takiar are both from the same field of endeavor, the purpose disclosed by Takiar would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 29, Applicant's Prior Art discloses the following:

a) the first and second chips are approximately the same size (See Figure 1).

10. Claim 30 is rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art in view of Takiar et al. (U.S. Patent No. 5,495,398), LoBianco et al. (U.S. Patent No. 6,340,846), Fogal et al. (U.S. Patent No. 5,323,060) and Kuramochi (U.S. Patent No. 5,521,122).

In regards to claim 30, Applicant's Prior Art fails to disclose the following:

a) second attach layer is an inorganic material.

However, Kuramochi discloses the use of silicon dioxide (See Column 5 Lines 28-31). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of silicon dioxide as disclosed in Kuramochi because it is usable in accordance with a kind of material and hardening temperature for an insulating film (See Column 5 Lines 25-39).

Additionally, since Applicant's Prior Art and Kuramochi are both from the same field of endeavor, the purpose disclosed by Kuramochi would have been recognized in the pertinent art of Applicant's Prior Art.

*Conclusion*

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

  
**AMIR ZARABIAN**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**

ML  
March 27, 2003